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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/021,736	10/30/2001	Malcolm Whitlock	72404	1061

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EXAMINER	
MEEK, JACOB M	

ART UNIT	PAPER NUMBER
2637	

DATE MAILED: 09/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/021,736	WHITLOCK, MALCOLM	
	Examiner	Art Unit	
	Jacob Meek	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 4, 6, 7, 8, 10 -12, 14, 15, 17* is/are rejected.

7)☒ Claim(s) *5, 9, 13, 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in United States on 10/30/2001. It is noted, however, that applicant has not filed a certified copy of the United Kingdom application as required by 35 U.S.C. 119(b).

Response to Arguments

1. Applicant's arguments, see pages 6 - 8, filed June 23, 2005 with respect to Marz (US-5,923,706) have been fully considered and are persuasive. The rejection of claims 1, 2, 7, 8, and 15 has been withdrawn.

2. Applicant's arguments, see pages 10, 11, filed June 23, 2005 with respect to Naudet (US-6,377,644) and rejection of claim 9 have been fully considered and are persuasive. The rejection of claim 9 has been withdrawn.

3. Applicant's arguments, filed June 23, 2005 with respect to Naudet (US-6,377,644) and rejection of claims 1- 4, have been fully considered but they are not persuasive.

With regard to applicant's argument regarding Naudet's clock implementation (page 8) of claim 1, the difference being argued is not present in the claim, therefore Naudet's invention still discloses the use of a digital reference having a predetermined frequency offset from that of digital input signal (see column 2, lines 48 – 60).

With regard to applicant's argument regarding relationship between input signal and reference clock (page 8) of claim 1. Examiner notes that Naudet discloses setting measurement time and phase relationship of reference signal (see column 2, lines 48 – 60). Naudet does not appear to require a high speed clock, as his sampling is based on a single clock utilizing delay elements and therefore constitutes a digital reference signal. Examiner notes that applicant also samples, stores, and processes data, as does Naudet. Examiner further notes that "determining the time difference" does not specify a particular implementation as being argued.

With regard to applicant's argument regarding sampling (page 9). First, Naudet's invention samples incoming signal and stores data as does applicant and therefore can be considered equivalent. Second, claim 1 does not specify a direct readout of samples.

With regard to applicant's argument regarding samples, and periodic sequence (page 9). Determination of time difference is what Naudet ultimately analyzes with his system. While Naudet's implementation may differ from applicant's disclosure, it is interpreted as determining time differences between instances as stated in instant application.

With regard to applicant's regarding a specific phase relationship between reference clock and signal (page 9). Naudet discloses the setting of an initial phase relation between reference clock and signal, and collecting sets of samples (see column 2, lines 1 – 4). Naudet then shifts his reference clock and collects another set of data. Examiner interprets Naudet as reading on applicant's claim as Naudet does samples and determine the time variations with a 1st set of samples as in instant application.

With regard to applicant's argument generation of clock (page 9), Naudet discloses the ability to generate a digital reference clock. Applicant's claim does not require a particular

source and therefore Naudet is interpreted as providing a digital reference source as disclosed.

With regard to applicant's argument regarding the determining of frequency (page 10). Naudet discloses determining the frequency of data signal and then choosing a ratio so that the period is substantially the same (see column 2, lines 48 – 59). Applicant's claim does not specify a particular digital reference source.

With regard to applicant's argument regarding the sampling with respect to clock edge (see page 10). Naudet is clear on the sampling at fixed clock relationship and accumulating data. Naudet specifies sampling and collecting a set of data for a fixed clock relationship and detecting errors (see column 3, line 62 – column 4, line 5).

With regard to applicant's argument that Naudet utilizes a higher speed clock. Naudet specifically discloses the use of a lower frequency clock in order to reduce cost (see column 3, lines 45 – 52). Also, Naudet's disclosure also shows equal or lower frequency sample clocks (Figure 3A, and 4A). Naudet achieves his seemingly higher sampling rate by using phase shifted versions of his lower speed reference clock.

With regard to applicant's argument regarding claim programmable oscillator. Naudet discloses adjustment of his oscillator to a predetermined offset (see column 4, lines 34 – 36).

With regard to rejections of claims 14 and 15, as rejection of claims 7 and 8 is maintained so is the rejection of claims 14 and 15.

4. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., single phase clock, oscillator type) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the

specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

5. Restatement of previously rejected claims.

Claims 1 – 4, 7, 8, 10 - 12, and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Naudet (US Patent 6,377,644).

With regard to claim 1, Naudet discloses a method for measuring jitter in a digital signal (see column 1, lines 5 - 9) compromising producing a digital reference signal having a predetermined frequency offset from digital input signal (see column 1, lines 63 – 65), detecting a 1st occurrence of phase relationship between digital input signal and digital reference signal (see column 3, lines 62 – column 4, line 1 where this is interpreted as equivalent), detecting subsequent occurrence of predetermined phase relationship between digital input signal and digital reference signal (see column 4, lines 1 – 10), determining time difference between 1st and subsequent occurrence to determine a measurement of jitter present in digital input signal (see column 4, lines 64 – 67).

With regard to claim 2, Naudet discloses a method of producing a digital reference signal compromising measuring frequency of digital input signal to produce a frequency measurement (see column 6, lines 20 –30), and using frequency measurement to produce digital reference signal having a frequency which is offset by a predetermined amount (see column 6, lines 31 – 47 where this is interpreted as equivalent).

With regard to claim 3, Naudet discloses a method of detecting a 1st occurrence of a predetermined phase relationship between digital input signal and digital reference signal (see column 5, lines 1 – 14 where this is interpreted as equivalent) and the step of detecting subsequent occurrence of predetermined phase relationship between digital input signal and digital reference signal compromise detecting coincidence of similar edges of digital input signal and digital reference signal (see column 5, lines 6 – 28).

With regard to claim 4, Naudet discloses a method of detecting subsequent occurrence of predetermined phase relationship between digital input signal and digital reference signal comprises detecting over a plurality of subsequent occurrences a maximum time difference value and a minimum time difference value (see column 5, lines 15 – 28 where this is interpreted as being inclusive) and determining from maximum time difference value and minimum time difference value a total peak to peak jitter measurement (see column 5, lines 49 – 59 where calculation is interpreted as being inclusive of peak-peak measurement).

With regard to claims 7, 8, 11, and 12 Naudet discloses an apparatus incorporating the steps claimed as method in claims 1 – 4 respectively and therefore, it would have been obvious considering the aforementioned rejection of method claims of 1 – 4.

With regard to claim 10, Naudet discloses an apparatus wherein signal producing arrangement compromises a programmable oscillator (see column 6, lines 38 – 47 where this is interpreted as equivalent).

With regard to claim 15, Naudet discloses the apparatus is arranged to sense jitter in a telecommunications PCM signal (see column 1, lines 5 – 9 where this is interpreted as being inclusive of telecommunications PCM signals).

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Naudet ('644).

With regard to claim 14, Naudet discloses a digital measurement device. Naudet is silent with respect to his apparatus being implemented in an FPGA. It would have been obvious to one of ordinary skill of the art at the time of invention the digital measurement device could be implemented in an FPGA as this represents one of commonly used digital design devices (PAL, ASIC, FPGA, etc).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 6 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Naudet (US Patent 6,377,644).

With regard to claim 6, Naudet teaches a method for prescaling digital input signal to increase resolution of jitter measurement (see column 2, lines 34 – 52 and column 6, lines 30 – 36, where time pitch is interpreted as equivalent).

With regard to claims 17, Naudet discloses an apparatus incorporating the steps claimed as method in claim 6 and therefore, it would have been obvious considering the aforementioned rejection of method claim of 6.

Allowable Subject Matter

7. Claims 5, 9, 13, and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Other Cited Prior Art

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Smith (US-5,748,672), Wilstrup (US-6,356,850), and Nakayama (US-6,366,631) disclose variations of jitter analysis. Ballatyne (US-2001/0044701) discloses jitter analysis with max / min capabilities.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Meek whose telephone number is (571)272-3013. The examiner can normally be reached on 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571)272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JMM
8/31/05

JAY K. PATEL
SUPERVISORY PATENT EXAMINER